

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	205	703/2.ccls. and @pd>"20061201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 12:19

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S44	1176	verilog and 'define and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:49
S45	3	"6813597".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:51
S46	3	"6401230".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:53
S47	2	"6226780".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:54
S48	2	"5841663".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:05
S49	2	"6,311,239".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:06
S50	2	"5802399".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:06
S51	114	yumoto.in. and @ad>"19980101" and @ad<"20010701"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:07

Scholar All articles - **Recent articles** Results 1 - 10 of about 1,500 for **verilog parameterized design**

All Results

[L Bening](#)

[E Girczyc](#)

[J Babb](#)

[D Fitzpatrick](#)

[S Carlson](#)

[\[book\] ... of Verifiable Rtl Design: A Functional Coding Style Supporting Verification Processes in Verilog - all 6 versions »](#)

L Bening - 2001 - books.google.com

... 2. Verilog (Computer hardware description language) 3. Electronic digital ... 6.4.2 Model Checking and Parameterized Modules 126 6.4 ... 131 7. 1 Design Content 132 7. 1 ...

[Cited by 54](#) - [Related Articles](#) - [Web Search](#) - [Library Search](#)

[VHDL & Verilog Compared & Contrasted-Plus Modeled Example Written in VHDL, Verilog and C. - all 16 versions »](#)

DJ Smith - Proc. 33rd Design Automation Conf, 1996 - doi.ieeecomputersociety.org

... reuse, • configuration statements for configuring design structure, • generate ... Verilog. ... to parameterize models by overloading parameter constants, there is ...

[Cited by 25](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Verischemelog: Verilog embedded in Scheme - all 4 versions »](#)

J Jennings, E Beuscher - Proceedings of the 2nd conference on Domain-specific ..., 2000 - portal.acm.org

... Verilog has a small macro language, essentially based ... Therefore, although many designs

are parameterized, there are ... Common design elements in digital systems ...

[Cited by 8](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Parameterized IP core design](#)

Z Junchao, C Weiliang, W Shaojun - ASIC, 2001. Proceedings. 4th International Conference on, 2001 - ieeexplore.ieee.org

... They are common in the design of the control Page 3 ... needs IF providers to support both Verilog and VFIDL ... For example, a parameterized IF core is designed to ...

[Cited by 9](#) - [Related Articles](#) - [Web Search](#)

[Increasing design quality and engineering productivity through design reuse - all 2 versions »](#)

E Girczyc, S Carlson - Proceedings of the 30th international conference on Design ..., 1993 - portal.acm.org

... Next, designs can be parameterized. While a ... In an FILD methodology, functionality can also be parameterized without increasing design cost if ...

[Cited by 43](#) - [Related Articles](#) - [Web Search](#)

[Three decades of HDLs. II. Conlan through Verilog - all 6 versions »](#)

D Borrione, R Piloty, D Hill, KJ Lieberherr, P ... - Design & Test of Computers, IEEE, 1992 - ieeexplore.ieee.org

... in the mid-1 970s through the development of Verilog in the ... evaluate and write assertions either after the interface/ parameter list of a design entity or ...

[Cited by 9](#) - [Related Articles](#) - [Web Search](#)

[Trends in CAD of analog ICs - all 2 versions »](#)

BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org

... New develop- ments in AHDs have seen the emergence of standards for VHDL-A and **Verilog-A** to ... Model **parameter** extraction and **design** methodologies Inadequate ...
[Cited by 15](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[AHD languages-a must for time-critical designs - all 3 versions »](#)

BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - [ieeexplore.ieee.org](#)

... to be repre- sented, VHDL-A and **Verilog-A** are lan ... is some flexibility to specify the **parameter** values such ... application areas of the analog **design** process where ...

[Cited by 7](#) - [Related Articles](#) - [Web Search](#)

[Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - all 9 versions »](#)

CE Cummings - SNUG-2001 San Jose, CA Voted Best paper, 2001 - [sunburst-design.com](#)

... This time window is specified as a **design parameter** precisely to keep a data signal from changing too close to another synchronizing signal that could cause ...

[Cited by 8](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[A System for Evaluating Performance and Cost of SIMD Array Designs - all 14 versions »](#)

MC Herbordt, J Cravy, R Sam, O Kidwai, C Lin - Journal of Parallel and Distributed Computing, 2000 - Elsevier

... program to generate the **designs** in the **Verilog** high-level ... 4. If a **design** to be evaluated has not ... thesized, but is legal for the **parameterized** hardware model ...

[Cited by 7](#) - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Google

Result Page: 1 2 3 4 5 6 7 8 9 10 [Next](#)

verilog parameterized design

Search

[Google Home](#) - [About Google](#) - [About Google Scholar](#)

©2007 Google

[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

verilog parameterized design

Search Patents

[Advanced Patent Search](#)
[Google Patent Search](#)

Filing date

☐ Return patents filed anytime☒ Return patents filed between Jan 1988 and Dec 2001

Patents

Patents 1 - 10 on verilog parameterized design. (0.27 seconds)

Apparatus and method for synthesizing integrated circuits using parameterized HDL modules ...

US Pat. 5841663 - Filed Sep 14, 1995 - VLSI Technology, Inc.

Kim ("Automatic behavioral Verilog model generation using engineering ... ("Guided synthesis and formal verification techniques for parameterized hardware ...

Method of generating customized megafunctions

US Pat. 6401230 - Filed Feb 1, 1999 - Altera Corporation

To the design compiler, parameterized ... a non-parameterized functions of a type that may be easily handled (by, for example, VHDL and Verilog compilers). ...

Electronic design automation apparatus and method utilizing a physical information database

US Pat. 5487018 - Filed Aug 13, 1993 - VLSI Technology, Inc.

This invention more particularly relates to an electronic design automation ... for the simple non-parameterized datapath cells typically used in the past. ...

FPGA modules parameterized by expressions

US Pat. 6216258 - Filed Mar 27, 1998 - Xilinx, Inc.

... hardware design languages (hdl) are similar to high level programming ... hdl such as VHDL or Verilog, and commonly used hlls such as C++ or Java. ...

Circuit design method and apparatus supporting a plurality of hardware design languages

US Pat. 6226780 - Filed Aug 31, 1998 - Mentor Graphics Corporation

... From Parameterized Schematic Design System," IEEE, pp. 130-134, 1997.* Sauge et al., "Integrating of Verilog-HDL and VHDL Languages in the SMASH™ ...

Method and apparatus for data path circuit layout design and memory medium for causing computer ...

US Pat. 5737237 - Filed Feb 16, 1996 - Matsushita Electric Industrial Co., Ltd.

14 is a flow chart of a data path circuit layout design SIS. ... language Verilog

HDL: The following description will discuss a parameterized function ...

Mixed signal synthesis behavioral models and use in circuit design optimization

US Pat. 6637018 - Filed Oct 26, 2000 - Cadence Design Systems, Inc.

25 vi- Generate the parameterized model. This task has to be executed first.

2-2-1 Synthesis Models design knowledge into a Synthesis Plan. ...

Method and apparatus for addressing multiple frame buffers

US Pat. 6411302 - Filed Jan 6, 1999 - Concise Multimedia and Communications Inc.

In VHDL a standard library of parameterized modules (LPM) is available. ...

components that can also be used to implement the current embodiment is Verilog. ...

Mixed signal synthesis

US Pat. 6813597 - Filed Jun 8, 2000 - Cadence Design Systems, Inc.

2.2.1 Synthesis Models 2. Model each performance characteristic in terms of design ...

US Pat. 6496962 - Filed Nov 17, 2000 - LSI Logic Corporation

The **Verilog** models may then be distributed as part of an ASIC design system. ...

Result Page: **1** 2 3 4 5 6 7 8 9 10 **Next**

Search Patents

[Google Home](#) - [About Google](#) - [About Google Patent Search](#)

©2007 Google

Search Results

[BROWSE](#)

[SEARCH](#)

[IEEE XPLORE GUIDE](#)

Results for "(parameterized design) <and> (pyr >= 1913 <and> pyr <= 2001)"

Your search matched 39 of 1589326 documents.

A maximum of 250 results are displayed, 25 to a page, sorted by Relevance in Descending order.


 [e-mail](#)

» **Search Options**

[View Session History](#)

[New Search](#)

» **Key**

	Indicates full text access
IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

(parameterized design) <and> (pyr >= 1913 <and> pyr <= 2001)

Search 

☐ Check to search only within this results set

Display Format: ☒ Citation ☐ Citation & Abstract

[view selected items](#)

[Select All](#) [Deselect All](#)

- ☐ 1. **Dimension-driven parameterized design of free form objects**
Yu, K.M.; Zhu, W.M.;
[Geometric Modeling and Processing 2000. Theory and Applications. Proceedings](#)
10-12 April 2000 Page(s):90 - 100
Digital Object Identifier 10.1109/GMAP.2000.838241
[Abstract](#) | Full Text: [PDF\(252 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)
- ☐ 2. **MIMO design models and internal regulators for cyclicly switched parameter-adaptive contro**
Morse, A.S.; Pait, F.M.;
[Automatic Control. IEEE Transactions on](#)
Volume 39, Issue 9, Sept. 1994 Page(s):1809 - 1818
Digital Object Identifier 10.1109/9.317097
[Abstract](#) | Full Text: [PDF\(876 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)
- ☐ 3. **Managing design patterns in MAKE style**
Tokuda, H.; Miura, T.;
[Communications. Computers and signal Processing. 2001. PACRIM. 2001 IEEE Pacific Rim Confe](#)
Volume 2, 26-28 Aug. 2001 Page(s):409 - 412 vol.2
Digital Object Identifier 10.1109/PACRIM.2001.953656
[Abstract](#) | Full Text: [PDF\(344 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)
- ☐ 4. **Proceedings Geometric Modeling and Processing 2000. Theory and Applications**
[Geometric Modeling and Processing 2000. Theory and Applications. Proceedings](#)
10-12 April 2000
Digital Object Identifier 10.1109/GMAP.2000.838232
[Abstract](#) | Full Text: [PDF\(40 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)
- ☐ 5. **A systematic analysis of reuse strategies for design of electronic circuits**
Koegst, M.; Conradi, P.; Garte, D.; Wahl, M.;
[Design. Automation and Test in Europe. 1998. Proceedings](#)
23-26 Feb. 1998 Page(s):292 - 296
Digital Object Identifier 10.1109/DATE.1998.655871
[Abstract](#) | Full Text: [PDF\(32 KB\)](#) **IEEE CNF**

- ☐ **6. A computationally efficient approach to microwave circuit modeling of complex high temperature superconductor circuits**
Pond, J.M.;
[Applied Superconductivity, IEEE Transactions on](#)
Volume 7, Issue 2, Part 3, June 1997 Page(s):3052 - 3055
Digital Object Identifier 10.1109/77.621976
[Abstract](#) | Full Text: [PDF\(492 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)

- ☐ **7. Embedded computer architecture and automation**
Ramakrishna Rau, B.; Schlansker, M.S.;
[Computer](#)
Volume 34, Issue 4, April 2001 Page(s):75 - 81
Digital Object Identifier 10.1109/2.917544
[Abstract](#) | Full Text: [PDF\(384 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)

- ☐ **8. Schematic driven module generation for analog circuits with performance optimization and manufacturing considerations**
Naiknaware, R.; Fiez, T.;
[Custom Integrated Circuits Conference, 1998., Proceedings of the IEEE 1998](#)
11-14 May 1998 Page(s):481 - 484
Digital Object Identifier 10.1109/CICC.1998.695023
[Abstract](#) | Full Text: [PDF\(492 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **9. The CARE toolset for developing verified programs from formal specifications**
Hemer, D.; Lindsay, P.;
[Assessment of Software Tools, 1996., Proceedings of the Fourth International Symposium on](#)
22-24 May 1996 Page(s):24 - 35
Digital Object Identifier 10.1109/AST.1996.506475
[Abstract](#) | Full Text: [PDF\(876 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **10. An interactive graphical approach to module generator development**
Lacroix, D.; Menkis, S.;
[Custom Integrated Circuits Conference, 1990., Proceedings of the IEEE 1990](#)
13-16 May 1990 Page(s):30.1/1 - 30.1/5
Digital Object Identifier 10.1109/CICC.1990.124833
[Abstract](#) | Full Text: [PDF\(284 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **11. Automatic verification of finite-state concurrent systems**
Clarke, E.M., Jr.;
[Logic in Computer Science, 1994, LICS '94, Proceedings., Symposium on](#)
4-7 July 1994 Page(s):126
Digital Object Identifier 10.1109/LICS.1994.316079
[Abstract](#) | Full Text: [PDF\(52 KB\)](#) **IEEE CNF**
[Rights and Permissions](#)

- ☐ **12. System level hardware module generation**
Srivastava, M.B.; Brodersen, R.W.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 3, Issue 1, March 1995 Page(s):20 - 35
Digital Object Identifier 10.1109/92.365451
[Abstract](#) | Full Text: [PDF\(1732 KB\)](#) **IEEE JNL**
[Rights and Permissions](#)